

# SSD1306

## *Advance Information*

### **128 x 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SSD1306

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## 1 GENERAL DESCRIPTION

SSD1306 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1306 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface, I<sup>2</sup>C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

## 2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
  - V<sub>DD</sub> = 1.65V to 3.3V for IC logic
  - V<sub>CC</sub> = 7V to 15V for Panel driving
- For matrix display
  - OLED driving output voltage, 15V maximum
  - Segment maximum source current: 100uA
  - Common maximum sink current: 15mA
  - 256 step contrast brightness current control
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - 3 /4 wire Serial Peripheral Interface
  - I<sup>2</sup>C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG & COF
- Wide range of operating temperature: -40°C to 85°C

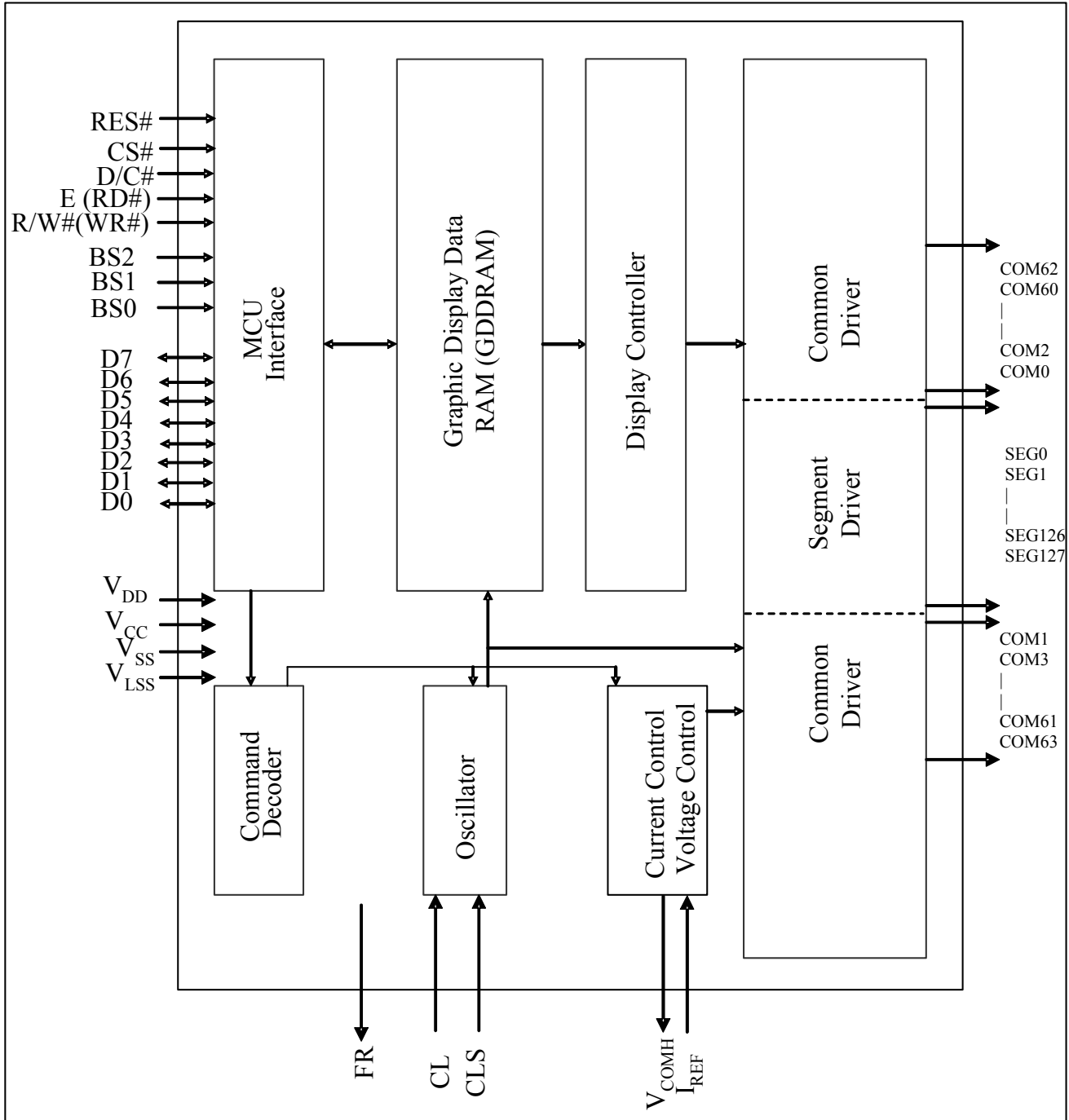
## 3 ORDERING INFORMATION

**Table 3-1: Ordering Information**

| Ordering Part Number | SEG | COM | Package Form | Reference | Remark  |
|----------------------|-----|-----|--------------|-----------|---|
| SSD1306Z             | 128 | 64  | COG          | 8         | <ul style="list-style-type: none"> <li>○ Min SEG pad pitch : 47um</li> <li>○ Min COM pad pitch : 40um</li> <li>○ Die thickness: 300 +/- 25um</li> </ul>   |
| SSD1306TR1           | 104 | 48  | TAB          | 11, 56    | <ul style="list-style-type: none"> <li>○ 35mm film, 4 sprocket hole, Folding TAB</li> <li>○ 8-bit 80 / 8-bit 68 / SPI / I<sup>2</sup>C interface</li> <li>○ SEG, COM lead pitch 0.1mm x 0.997 =0.0997mm</li> <li>○ Die thickness: 457 +/- 25um</li> </ul> |

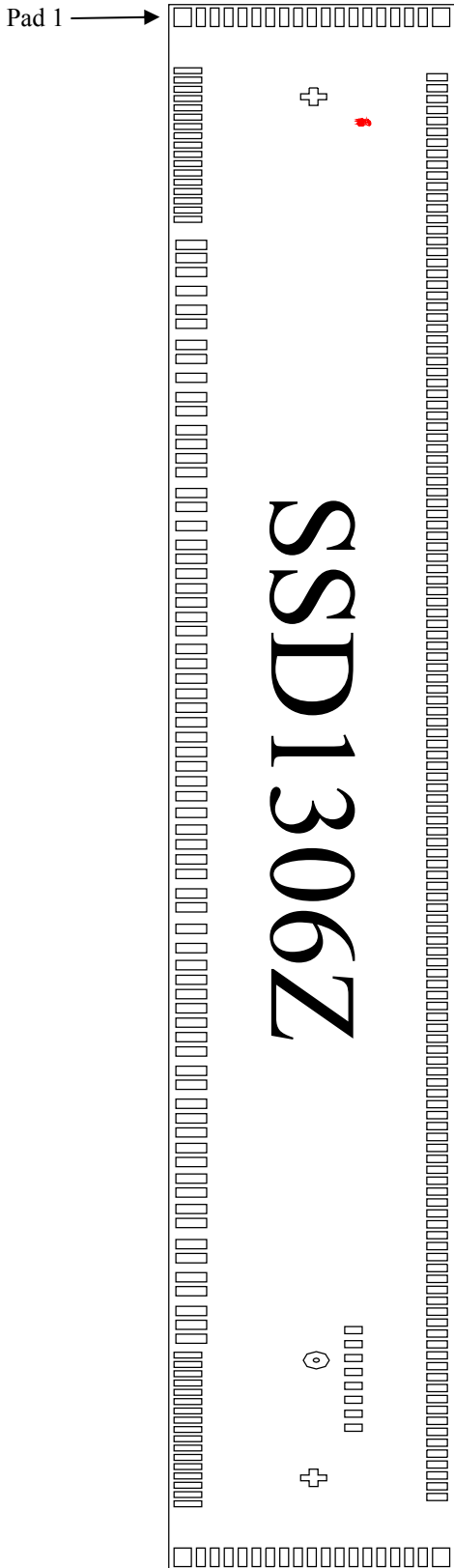
## 4 BLOCK DIAGRAM

Figure 4-1 SSD1306 Block Diagram



## 5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1306Z Die Drawing



|                   |                 |
|-------------------|-----------------|
| Die size          | 6.76mm x 0.86mm |
| Die thickness     | 300 +/- 25um    |
| Min I/O pad pitch | 60um            |
| Min SEG pad pitch | 47um            |
| Min COM pad pitch | 40um            |
| Bump height       | Nominal 15um    |

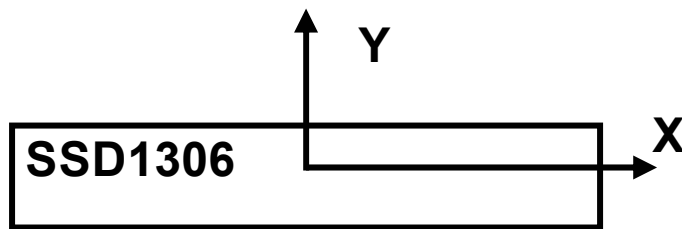
|                                    |             |
|------------------------------------|-------------|
| Bump size                          |             |
| Pad 1, 106, 124, 256               | 80um x 50um |
| Pad 2-18, 89-105, 107-123, 257-273 | 25um x 80um |
| Pad 19-88                          | 40um x 89um |
| Pad 125-255                        | 31um x 59um |
| Pad 274-281 (TR pads)              | 30um x 50um |

| Alignment mark | Position           | Size                |
|----------------|--------------------|---------------------|
| + shape        | (-2973, 0)         | 75um x 75um         |
| + shape        | (2973, 0)          | 75um x 75um         |
| Circle         | (2466.665, 7.575)  | R37.5um, inner 18um |
| SSL Logo       | (-2862.35, 144.82) | -                   |

(For details dimension please see p.9 )

### Note

- (1) Diagram showing the Gold bumps face up.
- (2) Coordinates are referenced to center of the chip.
- (3) Coordinate units and size of all alignment marks are in um.
- (4) All alignment keys do not contain gold

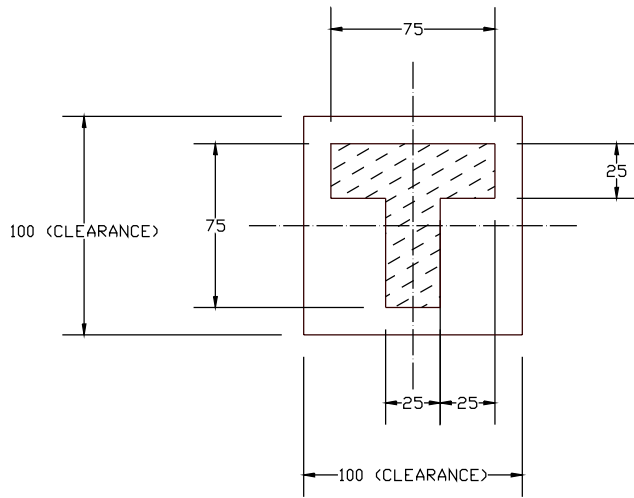


**Pad 1,2,3,...->281**

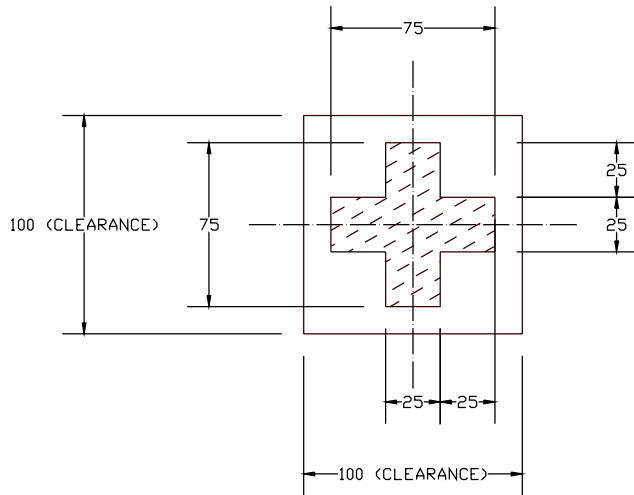
**Gold Bumps face up**



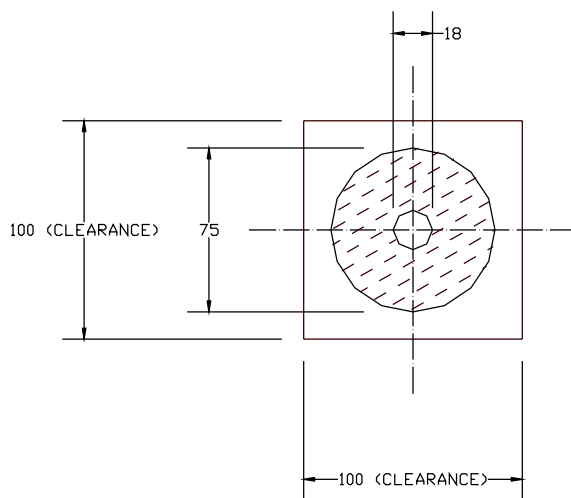
Figure 5-2 : SSD1306Z alignment mark dimensions



T shape



+ shape



Circle

\*All units are in um

**Table 5-1 : SSD1306Z Bump Die Pad Coordinates**

| Pad no. | Pad Name | X-pos     | Y-pos   |
|---------|----------|-----------|---------|
| 1       | NC       | -3315     | -377.5  |
| 2       | VSS      | -3084.77  | -362.5  |
| 3       | COM49    | -3044.77  | -362.5  |
| 4       | COM50    | -3004.77  | -362.5  |
| 5       | COM51    | -2964.77  | -362.5  |
| 6       | COM52    | -2924.77  | -362.5  |
| 7       | COM53    | -2884.77  | -362.5  |
| 8       | COM54    | -2844.77  | -362.5  |
| 9       | COM55    | -2804.77  | -362.5  |
| 10      | COM56    | -2764.77  | -362.5  |
| 11      | COM57    | -2724.77  | -362.5  |
| 12      | COM58    | -2684.77  | -362.5  |
| 13      | COM59    | -2644.77  | -362.5  |
| 14      | COM60    | -2604.77  | -362.5  |
| 15      | COM61    | -2564.77  | -362.5  |
| 16      | COM62    | -2524.77  | -362.5  |
| 17      | COM63    | -2484.77  | -362.5  |
| 18      | VCOMH    | -2444.77  | -362.5  |
| 19      | NC       | -2334.965 | -352.83 |
| 20      | C2P      | -2278.265 | -352.83 |
| 21      | C2P      | -2218.265 | -352.83 |
| 22      | C2N      | -2136.715 | -352.83 |
| 23      | C2N      | -2055.465 | -352.83 |
| 24      | C1P      | -1995.465 | -352.83 |
| 25      | C1P      | -1904.115 | -352.83 |
| 26      | C1N      | -1844.115 | -352.83 |
| 27      | C1N      | -1762.865 | -352.83 |
| 28      | VBAT     | -1679.31  | -352.83 |
| 29      | VBAT     | -1619.31  | -352.83 |
| 30      | VBREF    | -1537.51  | -352.83 |
| 31      | BGGND    | -1477.51  | -352.83 |
| 32      | VCC      | -1416.01  | -352.83 |
| 33      | VCC      | -1356.01  | -352.83 |
| 34      | VCOMH    | -1266.955 | -352.83 |
| 35      | VCOMH    | -1206.955 | -352.83 |
| 36      | VLSS     | -1125.155 | -352.83 |
| 37      | VLSS     | -1043.355 | -352.83 |
| 38      | VLSS     | -983.355  | -352.83 |
| 39      | VSS      | -920      | -352.83 |
| 40      | VSS      | -856      | -352.83 |
| 41      | VSS      | -796      | -352.83 |
| 42      | VDD      | -732.645  | -352.83 |
| 43      | VDD      | -672.645  | -352.83 |
| 44      | BS0      | -595.655  | -352.83 |
| 45      | VSS      | -531.955  | -352.83 |
| 46      | BS1      | -467.655  | -352.83 |
| 47      | VDD      | -403.155  | -352.83 |
| 48      | VDD      | -342.555  | -352.83 |
| 49      | BS2      | -279.705  | -352.83 |
| 50      | VSS      | -215.705  | -352.83 |
| 51      | FR       | -151.955  | -352.83 |
| 52      | CL       | -89.815   | -352.83 |
| 53      | VSS      | -25.665   | -352.83 |
| 54      | CS#      | 38.635    | -352.83 |
| 55      | RES#     | 109.835   | -352.83 |
| 56      | D/C#     | 182.425   | -352.83 |
| 57      | VSS      | 246.125   | -352.83 |
| 58      | R/W#     | 310.425   | -352.83 |
| 59      | E        | 373.125   | -352.83 |
| 60      | VDD      | 457.175   | -352.83 |
| 61      | VDD      | 517.175   | -352.83 |
| 62      | D0       | 609.275   | -352.83 |
| 63      | D1       | 692.475   | -352.83 |
| 64      | D2       | 765.675   | -352.83 |
| 65      | D3       | 828.875   | -352.83 |
| 66      | VSS      | 890.325   | -352.83 |
| 67      | D4       | 951.275   | -352.83 |
| 68      | D5       | 1013.315  | -352.83 |
| 69      | D6       | 1075.355  | -352.83 |
| 70      | D7       | 1137.395  | -352.83 |
| 71      | VSS      | 1220.735  | -352.83 |
| 72      | VSS      | 1280.735  | -352.83 |
| 73      | CLS      | 1362.585  | -352.83 |
| 74      | VDD      | 1425.285  | -352.83 |
| 75      | VDD      | 1485.885  | -352.83 |
| 76      | VDD      | 1553.185  | -352.83 |
| 77      | VDD      | 1613.185  | -352.83 |
| 78      | IREF     | 1684.585  | -352.83 |
| 79      | IREF     | 1744.585  | -352.83 |
| 80      | VCOMH    | 1815.585  | -352.83 |

| Pad no. | Pad Name | X-pos    | Y-pos   |
|---------|----------|----------|---------|
| 81      | VCOMH    | 1875.585 | -352.83 |
| 82      | VCC      | 1967.185 | -352.83 |
| 83      | VCC      | 2027.185 | -352.83 |
| 84      | VLSS     | 2109.185 | -352.83 |
| 85      | VLSS     | 2169.185 | -352.83 |
| 86      | VLSS     | 2254.185 | -352.83 |
| 87      | NC       | 2314.185 | -352.83 |
| 88      | NC       | 2374.185 | -352.83 |
| 89      | VSS      | 2444.77  | -362.5  |
| 90      | COM31    | 2484.77  | -362.5  |
| 91      | COM30    | 2524.77  | -362.5  |
| 92      | COM29    | 2564.77  | -362.5  |
| 93      | COM28    | 2604.77  | -362.5  |
| 94      | COM27    | 2644.77  | -362.5  |
| 95      | COM26    | 2684.77  | -362.5  |
| 96      | COM25    | 2724.77  | -362.5  |
| 97      | COM24    | 2764.77  | -362.5  |
| 98      | COM23    | 2804.77  | -362.5  |
| 99      | COM22    | 2844.77  | -362.5  |
| 100     | COM21    | 2884.77  | -362.5  |
| 101     | COM20    | 2924.77  | -362.5  |
| 102     | COM19    | 2964.77  | -362.5  |
| 103     | COM18    | 3004.77  | -362.5  |
| 104     | COM17    | 3044.77  | -362.5  |
| 105     | VSS      | 3084.77  | -362.5  |
| 106     | NC       | 3315     | -377.5  |
| 107     | COM16    | 3315     | -325    |
| 108     | COM15    | 3315     | -285    |
| 109     | COM14    | 3315     | -245    |
| 110     | COM13    | 3315     | -205    |
| 111     | COM12    | 3315     | -165    |
| 112     | COM11    | 3315     | -125    |
| 113     | COM10    | 3315     | -85     |
| 114     | COM9     | 3315     | -45     |
| 115     | COM8     | 3315     | -5      |
| 116     | COM7     | 3315     | 35      |
| 117     | COM6     | 3315     | 75      |
| 118     | COM5     | 3315     | 115     |
| 119     | COM4     | 3315     | 155     |
| 120     | COM3     | 3315     | 195     |
| 121     | COM2     | 3315     | 235     |
| 122     | COM1     | 3315     | 275     |
| 123     | COM0     | 3315     | 315     |
| 124     | NC       | 3315     | 367.5   |
| 125     | NC       | 3055.5   | 356     |
| 126     | SEG0     | 3009.5   | 356     |
| 127     | SEG1     | 2962.5   | 356     |
| 128     | SEG2     | 2915.5   | 356     |
| 129     | SEG3     | 2868.5   | 356     |
| 130     | SEG4     | 2821.5   | 356     |
| 131     | SEG5     | 2774.5   | 356     |
| 132     | SEG6     | 2727.5   | 356     |
| 133     | SEG7     | 2680.5   | 356     |
| 134     | SEG8     | 2633.5   | 356     |
| 135     | SEG9     | 2586.5   | 356     |
| 136     | SEG10    | 2539.5   | 356     |
| 137     | SEG11    | 2492.5   | 356     |
| 138     | SEG12    | 2445.5   | 356     |
| 139     | SEG13    | 2398.5   | 356     |
| 140     | SEG14    | 2351.5   | 356     |
| 141     | SEG15    | 2304.5   | 356     |
| 142     | SEG16    | 2257.5   | 356     |
| 143     | SEG17    | 2210.5   | 356     |
| 144     | SEG18    | 2163.5   | 356     |
| 145     | SEG19    | 2116.5   | 356     |
| 146     | SEG20    | 2069.5   | 356     |
| 147     | SEG21    | 2022.5   | 356     |
| 148     | SEG22    | 1975.5   | 356     |
| 149     | SEG23    | 1928.5   | 356     |
| 150     | SEG24    | 1881.5   | 356     |
| 151     | SEG25    | 1834.5   | 356     |
| 152     | SEG26    | 1787.5   | 356     |
| 153     | SEG27    | 1740.5   | 356     |
| 154     | SEG28    | 1693.5   | 356     |
| 155     | SEG29    | 1646.5   | 356     |
| 156     | SEG30    | 1599.5   | 356     |
| 157     | SEG31    | 1552.5   | 356     |
| 158     | SEG32    | 1505.5   | 356     |
| 159     | SEG33    | 1458.5   | 356     |
| 160     | SEG34    | 1411.5   | 356     |

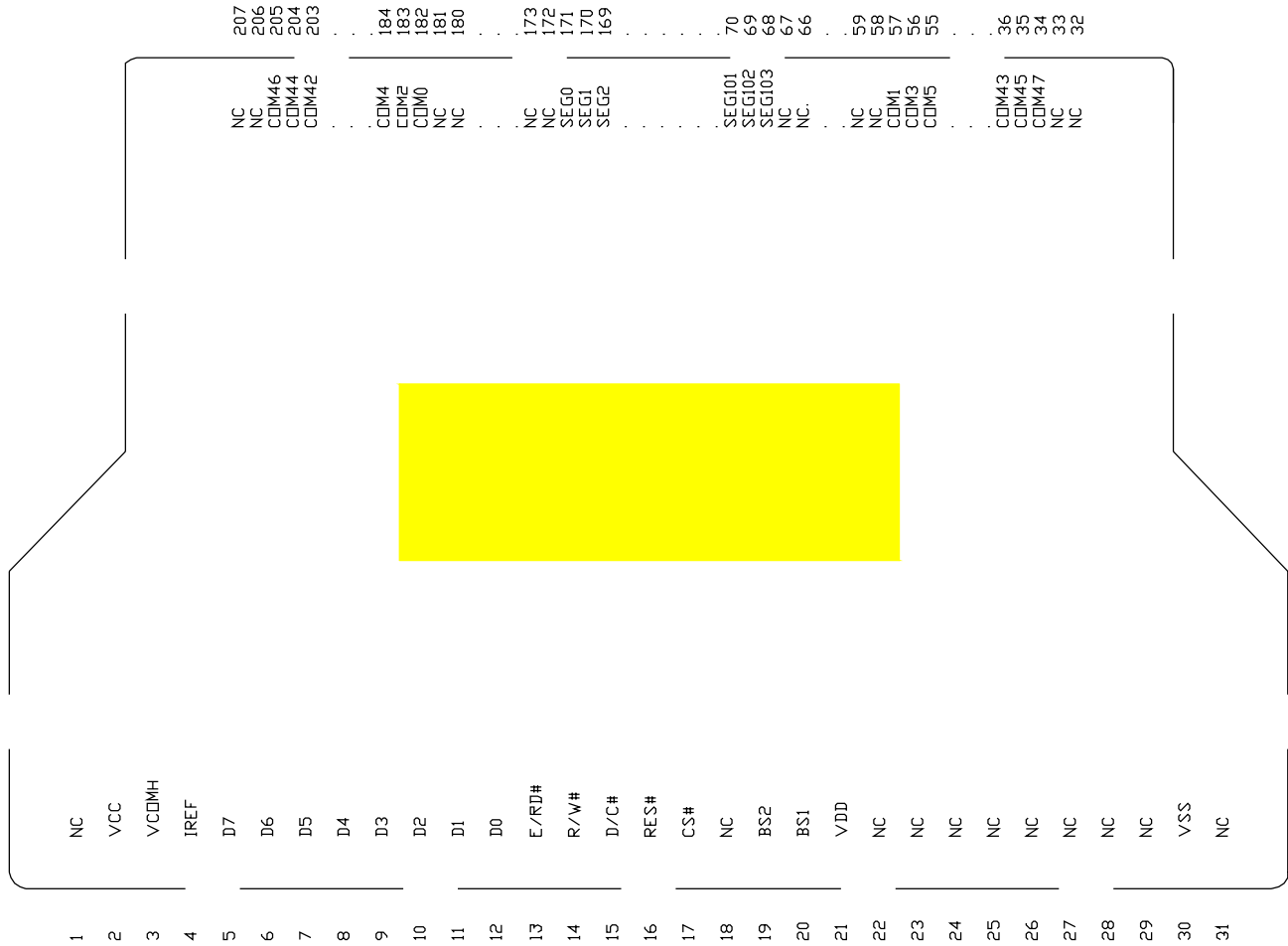
| Pad no. | Pad Name | X-pos   | Y-pos |
|---------|----------|---------|-------|
| 161     | SEG35    | 1364.5  | 356   |
| 162     | SEG36    | 1317.5  | 356   |
| 163     | SEG37    | 1270.5  | 356   |
| 164     | SEG38    | 1223.5  | 356   |
| 165     | SEG39    | 1176.5  | 356   |
| 166     | SEG40    | 1129.5  | 356   |
| 167     | SEG41    | 1082.5  | 356   |
| 168     | SEG42    | 1035.5  | 356   |
| 169     | SEG43    | 988.5   | 356   |
| 170     | SEG44    | 941.5   | 356   |
| 171     | SEG45    | 894.5   | 356   |
| 172     | SEG46    | 847.5   | 356   |
| 173     | SEG47    | 800.5   | 356   |
| 174     | SEG48    | 753.5   | 356   |
| 175     | SEG49    | 706.5   | 356   |
| 176     | SEG50    | 659.5   | 356   |
| 177     | SEG51    | 612.5   | 356   |
| 178     | SEG52    | 565.5   | 356   |
| 179     | SEG53    | 518.5   | 356   |
| 180     | SEG54    | 471.5   | 356   |
| 181     | SEG55    | 424.5   | 356   |
| 182     | SEG56    | 377.5   | 356   |
| 183     | SEG57    | 330.5   | 356   |
| 184     | SEG58    | 283.5   | 356   |
| 185     | SEG59    | 236.5   | 356   |
| 186     | SEG60    | 189.5   | 356   |
| 187     | SEG61    | 142.5   | 356   |
| 188     | SEG62    | 95.5    | 356   |
| 189     | SEG63    | 48.5    | 356   |
| 190     | SEG64    | 1.5     | 356   |
| 191     | SEG65    | -45.5   | 356   |
| 192     | SEG66    | -92.5   | 356   |
| 193     | SEG67    | -139.5  | 356   |
| 194     | SEG68    | -186.5  | 356   |
| 195     | SEG69    | -233.5  | 356   |
| 196     | SEG70    | -280.5  | 356   |
| 197     | SEG71    | -327.5  | 356   |
| 198     | SEG72    | -374.5  | 356   |
| 199     | SEG73    | -421.5  | 356   |
| 200     | SEG74    | -468.5  | 356   |
| 201     | SEG75    | -515.5  | 356   |
| 202     | SEG76    | -562.5  | 356   |
| 203     | SEG77    | -609.5  | 356   |
| 204     | SEG78    | -656.5  | 356   |
| 205     | SEG79    | -703.5  | 356   |
| 206     | SEG80    | -750.5  | 356   |
| 207     | SEG81    | -797.5  | 356   |
| 208     | SEG82    | -844.5  | 356   |
| 209     | SEG83    | -891.5  | 356   |
| 210     | NC       | -940    | 356   |
| 211     | SEG84    | -988.5  | 356   |
| 212     | SEG85    | -1035.5 | 356   |
| 213     | SEG86    | -1082.5 | 356   |
| 214     | SEG87    | -1129.5 | 356   |
| 215     | SEG88    | -1176.5 | 356   |
| 216     | SEG89    | -1223.5 | 356   |
| 217     | SEG90    | -1270.5 | 356   |
| 218     | SEG91    | -1317.5 | 356   |
| 219     | SEG92    | -1364.5 | 356   |
| 220     | SEG93    | -1411.5 | 356   |
| 221     | SEG94    | -1458.5 | 356   |
| 222     | SEG95    | -1505.5 | 356   |
| 223     | SEG96    | -1552.5 | 356   |
| 224     | SEG97    | -1599.5 | 356   |
| 225     | SEG98    | -1646.5 | 356   |
| 226     | SEG99    | -1693.5 | 356   |
| 227     | SEG100   | -1740.5 | 356   |
| 228     | SEG101   | -1787.5 | 356   |
| 229     | SEG102   | -1834.5 | 356   |
| 230     | SEG103   | -1881.5 | 356   |
| 231     | SEG104   | -1928.5 | 356   |
| 232     | SEG105   | -1975.5 | 356   |
| 233     | SEG106   | -2022.5 | 356   |
| 234     | SEG107   | -2069.5 | 356   |
| 235     | SEG108   | -2116.5 | 356   |
| 236     | SEG109   | -2163.5 | 356   |
| 237     | SEG110   | -2210.5 | 356   |
| 238     | SEG111   | -2257.5 | 356   |
| 239     | SEG112   | -2304.5 | 356   |
| 240     | SEG113   | -2351.5 | 356   |

| Pad no. | Pad Name | X-pos   | Y-pos |
|---------|----------|---------|-------|
| 241     | SEG114   | -2398.5 | 356   |
| 242     | SEG115   | -2445.5 | 356   |
| 243     | SEG116   | -2492.5 | 356   |
| 244     | SEG117   | -2539.5 | 356   |
| 245     | SEG118   | -2586.5 | 356   |
| 246     | SEG119   | -2633.5 | 356   |
| 247     | SEG120   | -2680.5 | 356   |
| 248     | SEG121   | -2727.5 | 356   |
| 249     | SEG122   | -2774.5 | 356   |
| 250     | SEG123   | -2821.5 | 356   |
| 251     | SEG124   | -2868.5 | 356   |
| 252     | SEG125   | -2915.5 | 356   |
| 253     | SEG126   | -2962.5 | 356   |
| 254     | SEG127   | -3009.5 | 356   |
| 255     | NC       | -3056.5 | 356   |
| 256     | NC       | -3315   | 367.5 |
| 257     | COM32    | -3315   | 315   |
| 258     | COM33    | -3315   | 275   |
| 259     | COM34    | -3315   | 235   |
| 260     | COM35    | -3315   | 195   |
| 261     | COM36    | -3315   | 155   |
| 262     | COM37    | -3315   | 115   |
| 263     | COM38    | -3315   | 75    |
| 264     | COM39    | -3315   | 35    |
| 265     | COM40    | -3315   | -5    |
| 266     | COM41    | -3315   | -45   |
| 267     | COM42    | -3315   | -85   |
| 268     | COM43    | -3315   | -125  |
| 269     | COM44    | -3315   | -165  |
| 270     | COM45    | -3315   | -205  |
| 271     | COM46    | -3315   | -245  |
| 272     | COM47    | -3315   | -285  |
| 273     | COM48    | -3315   | -325  |
| Pad no. | Pad Name | X-pos   | Y-pos |
| Pin#    | Pin name | X-dir   | Y-dir |
| 274     | TR0      | 2757.05 | 114.8 |
| 275     | TR1      | 2697.05 | 114.8 |
| 276     | TR2      | 2637.05 | 114.8 |
| 277     | TR3      | 2577.05 | 114.8 |
| 278     | VSS      | 2517.05 | 114.8 |
| 279     | TR4      | 2457.05 | 114.8 |
| 280     | TR5      | 2397.05 | 114.8 |
| 281     | TR6      | 2337.05 | 114.8 |

## 6 PIN ARRANGEMENT

### 6.1 SSD1306TR1 pin assignment

Figure 6-1 : SSD1306TR1 Pin Assignment



Note:

(1) COM sequence (Split) is under command setting: DAh, 12h

**Table 6-1 : SSD1306TR1 Pin Assignment Table**

| Pin no. | Pin Name | Pin no. | Pin Name | Pin no. | Pin Name |
|---------|----------|---------|----------|---------|----------|
| 1       | NC       | 81      | SEG90    | 161     | SEG10    |
| 2       | VCC      | 82      | SEG89    | 162     | SEG9     |
| 3       | VCOMH    | 83      | SEG88    | 163     | SEG8     |
| 4       | IREF     | 84      | SEG87    | 164     | SEG7     |
| 5       | D7       | 85      | SEG86    | 165     | SEG6     |
| 6       | D6       | 86      | SEG85    | 166     | SEG5     |
| 7       | D5       | 87      | SEG84    | 167     | SEG4     |
| 8       | D4       | 88      | SEG83    | 168     | SEG3     |
| 9       | D3       | 89      | SEG82    | 169     | SEG2     |
| 10      | D2       | 90      | SEG81    | 170     | SEG1     |
| 11      | D1       | 91      | SEG80    | 171     | SEG0     |
| 12      | D0       | 92      | SEG79    | 172     | NC       |
| 13      | E/RD#    | 93      | SEG78    | 173     | NC       |
| 14      | R/W#     | 94      | SEG77    | 174     | NC       |
| 15      | D/C#     | 95      | SEG76    | 175     | NC       |
| 16      | RES#     | 96      | SEG75    | 176     | NC       |
| 17      | CS#      | 97      | SEG74    | 177     | NC       |
| 18      | NC       | 98      | SEG73    | 178     | NC       |
| 19      | BS2      | 99      | SEG72    | 179     | NC       |
| 20      | BS1      | 100     | SEG71    | 180     | NC       |
| 21      | VDD      | 101     | SEG70    | 181     | NC       |
| 22      | NC       | 102     | SEG69    | 182     | COM0     |
| 23      | NC       | 103     | SEG68    | 183     | COM2     |
| 24      | NC       | 104     | SEG67    | 184     | COM4     |
| 25      | NC       | 105     | SEG66    | 185     | COM6     |
| 26      | NC       | 106     | SEG65    | 186     | COM8     |
| 27      | NC       | 107     | SEG64    | 187     | COM10    |
| 28      | NC       | 108     | SEG63    | 188     | COM12    |
| 29      | NC       | 109     | SEG62    | 189     | COM14    |
| 30      | VSS      | 110     | SEG61    | 190     | COM16    |
| 31      | NC       | 111     | SEG60    | 191     | COM18    |
| 32      | NC       | 112     | SEG59    | 192     | COM20    |
| 33      | NC       | 113     | SEG58    | 193     | COM22    |
| 34      | COM47    | 114     | SEG57    | 194     | COM24    |
| 35      | COM45    | 115     | SEG56    | 195     | COM26    |
| 36      | COM43    | 116     | SEG55    | 196     | COM28    |
| 37      | COM41    | 117     | SEG54    | 197     | COM30    |
| 38      | COM39    | 118     | SEG53    | 198     | COM32    |
| 39      | COM37    | 119     | SEG52    | 199     | COM34    |
| 40      | COM35    | 120     | SEG51    | 200     | COM36    |
| 41      | COM33    | 121     | SEG50    | 201     | COM38    |
| 42      | COM31    | 122     | SEG49    | 202     | COM40    |
| 43      | COM29    | 123     | SEG48    | 203     | COM42    |
| 44      | COM27    | 124     | SEG47    | 204     | COM44    |
| 45      | COM25    | 125     | SEG46    | 205     | COM46    |
| 46      | COM23    | 126     | SEG45    | 206     | NC       |
| 47      | COM21    | 127     | SEG44    | 207     | NC       |
| 48      | COM19    | 128     | SEG43    |         |          |
| 49      | COM17    | 129     | SEG42    |         |          |
| 50      | COM15    | 130     | SEG41    |         |          |
| 51      | COM13    | 131     | SEG40    |         |          |
| 52      | COM11    | 132     | SEG39    |         |          |
| 53      | COM9     | 133     | SEG38    |         |          |
| 54      | COM7     | 134     | SEG37    |         |          |
| 55      | COM5     | 135     | SEG36    |         |          |
| 56      | COM3     | 136     | SEG35    |         |          |
| 57      | COM1     | 137     | SEG34    |         |          |
| 58      | NC       | 138     | SEG33    |         |          |
| 59      | NC       | 139     | SEG32    |         |          |
| 60      | NC       | 140     | SEG31    |         |          |
| 61      | NC       | 141     | SEG30    |         |          |
| 62      | NC       | 142     | SEG29    |         |          |
| 63      | NC       | 143     | SEG28    |         |          |
| 64      | NC       | 144     | SEG27    |         |          |
| 65      | NC       | 145     | SEG26    |         |          |
| 66      | NC       | 146     | SEG25    |         |          |
| 67      | NC       | 147     | SEG24    |         |          |
| 68      | SEG103   | 148     | SEG23    |         |          |
| 69      | SEG102   | 149     | SEG22    |         |          |
| 70      | SEG101   | 150     | SEG21    |         |          |
| 71      | SEG100   | 151     | SEG20    |         |          |
| 72      | SEG99    | 152     | SEG19    |         |          |
| 73      | SEG98    | 153     | SEG18    |         |          |
| 74      | SEG97    | 154     | SEG17    |         |          |
| 75      | SEG96    | 155     | SEG16    |         |          |
| 76      | SEG95    | 156     | SEG15    |         |          |
| 77      | SEG94    | 157     | SEG14    |         |          |
| 78      | SEG93    | 158     | SEG13    |         |          |
| 79      | SEG92    | 159     | SEG12    |         |          |
| 80      | SEG91    | 160     | SEG11    |         |          |

## 7 PIN DESCRIPTION

### Key:

|                                     |                                |
|-------------------------------------|--------------------------------|
| I = Input                           | NC = Not Connected             |
| O = Output                          | Pull LOW= connect to Ground    |
| I/O = Bi-directional (input/output) | Pull HIGH= connect to $V_{DD}$ |
| P = Power pin                       |                                |

Figure 7-1 Pin Description

| Pin Name           | Type | Description   |
|--------------------|------|---|
| $V_{DD}$           | P    | Power supply pin for core logic operation.  |
| $V_{CC}$           | P    | Power supply for panel driving voltage. This is also the most positive power voltage supply pin.  |
| $V_{SS}$           | P    | This is a ground pin.   |
| $V_{LSS}$          | P    | This is an analog ground pin. It should be connected to $V_{SS}$ externally.  |
| $V_{COMH}$         | O    | The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and $V_{SS}$ .  |
| $V_{BAT}$          | P    | Reserved pin. It should be connected to $V_{DD}$ .  |
| BGGND              | P    | Reserved pin. It should be connected to ground.   |
| C1P/C1N<br>C2P/C2N | I    | Reserved pin. It should be kept NC.   |
| $V_{BREF}$         | P    | Reserved pin. It should be kept NC.   |
| BS[2:0]            | I    | MCU bus interface selection pins. Please refer to <b>Table 7-1</b> for the details of setting.  |
| $I_{REF}$          | I    | This is segment output current reference pin. A resistor should be connected between this pin and $V_{SS}$ to maintain the $I_{REF}$ current at 12.5 $\mu$ A. Please refer to <b>Figure 8-15</b> for the details of resistor value.                         |
| FR                 | O    | This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used. Please refer to Section <b>8.4</b> for details usage. |
| CL                 | I    | This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to $V_{SS}$ . When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin. |
| CLS                | I    | This is internal clock enable pin. When it is pulled HIGH (i.e. connect to $V_{DD}$ ), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.     |
| RES#               | I    | This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to $V_{DD}$ ) during normal operation.   |
| CS#                | I    | This pin is the chip select input. (active LOW).  |

| Pin Name      | Type | Description  |
|---------------|------|--|
| D/C#          | I    | This is Data/Command control pin. When it is pulled HIGH (i.e. connect to V <sub>DD</sub> ), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register.<br>In I <sup>2</sup> C mode, this pin acts as SA0 for slave address selection.<br>When 3-wire serial interface is selected, this pin must be connected to V <sub>SS</sub> .<br><br>For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams: <b>Figure 13-1</b> to <b>Figure 13-5</b> .                                    |
| E (RD#)       | I    | When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V <sub>DD</sub> ) and the chip is selected.<br>When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.<br>When serial or I <sup>2</sup> C interface is selected, this pin must be connected to V <sub>SS</sub> .  |
| R/W#(WR#)     | I    | This is read / write control input pin connecting to the MCU interface.<br>When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V <sub>DD</sub> ) and write mode when LOW.<br>When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.<br>When serial or I <sup>2</sup> C interface is selected, this pin must be connected to V <sub>SS</sub> . |
| D[7:0]        | IO   | These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.<br>When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC.<br>When I <sup>2</sup> C mode is selected, D2, D1 should be tied together and serve as SDA <sub>out</sub> , SDA <sub>in</sub> in application and D0 is the serial clock input, SCL.   |
| TR0-TR6       | -    | Testing reserved pins. It should be kept NC.   |
| SEG0 ~ SEG127 | O    | These pins provide Segment switch signals to OLED panel. These pins are V <sub>SS</sub> state when display is OFF.   |
| COM0 ~ COM63  | O    | These pins provide Common switch signals to OLED panel. They are in high impedance state when display is OFF.  |
| NC            | -    | This is dummy pin. Do not group or short NC pins together.   |

**Table 7-1 : MCU Bus Interface Pin Selection**

| SSD1306 Pin Name | I <sup>2</sup> C Interface | 6800-parallel interface (8 bit) | 8080-parallel interface (8 bit) | 4-wire Serial interface | 3-wire Serial interface |
|------------------|----------------------------|---------------------------------|---------------------------------|-------------------------|-------------------------|
| BS0              | 0                          | 0                               | 0                               | 0                       | 1                       |
| BS1              | 1                          | 0                               | 1                               | 0                       | 0                       |
| BS2              | 0                          | 1                               | 1                               | 0                       | 0                       |

**Note**

<sup>(1)</sup> 0 is connected to V<sub>SS</sub>

<sup>(2)</sup> 1 is connected to V<sub>DD</sub>

## 8 FUNCTIONAL BLOCK DESCRIPTIONS

### 8.1 MCU Interface selection

SSD1306 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-1 for BS[2:0] setting).

**Table 8-1 : MCU interface assignment under different bus interface mode**

| Pin Name<br>Bus Interface | Data/Command Interface |    |    |    |                    |                   |      |         | Control Signal |      |         |      |      |
|---------------------------|------------------------|----|----|----|--------------------|-------------------|------|---------|----------------|------|---------|------|------|
|                           | D7                     | D6 | D5 | D4 | D3                 | D2                | D1   | D0      | E              | R/W# | CS#     | D/C# | RES# |
| 8-bit 8080                | D[7:0]                 |    |    |    |                    |                   |      |         | RD#            | WR#  | CS#     | D/C# | RES# |
| 8-bit 6800                | D[7:0]                 |    |    |    |                    |                   |      |         | E              | R/W# | CS#     | D/C# | RES# |
| 3-wire SPI                | Tie LOW                |    |    |    | NC                 | SDIN              | SCLK | Tie LOW |                | CS#  | Tie LOW | RES# |      |
| 4-wire SPI                | Tie LOW                |    |    |    | NC                 | SDIN              | SCLK | Tie LOW |                | CS#  | D/C#    | RES# |      |
| I <sup>2</sup> C          | Tie LOW                |    |    |    | SDA <sub>OUT</sub> | SDA <sub>IN</sub> | SCL  | Tie LOW |                |      | SA0     | RES# |      |

#### 8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

**Table 8-2 : Control pins of 6800 interface**

| Function      | E | R/W# | CS# | D/C# |
|---------------|---|------|-----|------|
| Write command | ↓ | L    | L   | L    |
| Read status   | ↓ | H    | L   | L    |
| Write data    | ↓ | L    | L   | H    |
| Read data     | ↓ | H    | L   | H    |

#### Note

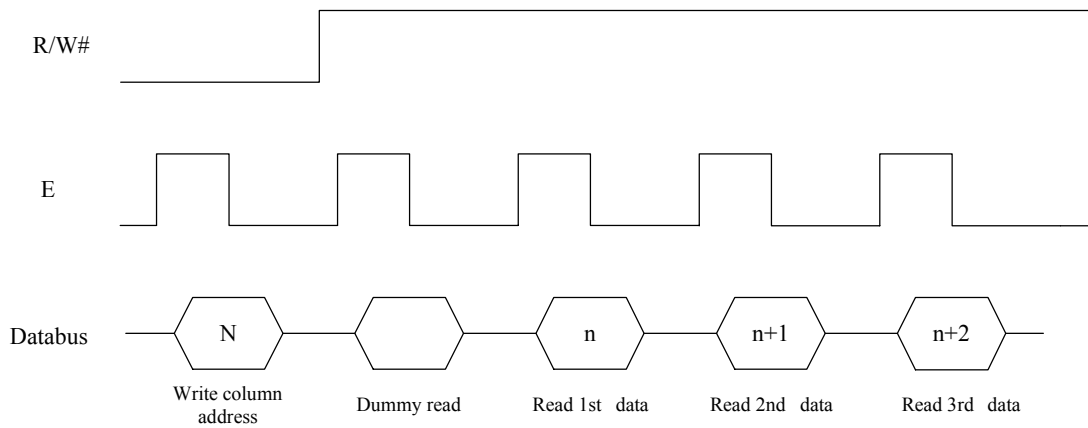
<sup>(1)</sup> ↓ stands for falling edge of signal

H stands for HIGH in signal

L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

**Figure 8-1 : Data read back procedure - insertion of dummy read**



### 8.1.2 MCU Parallel 8080-series Interface

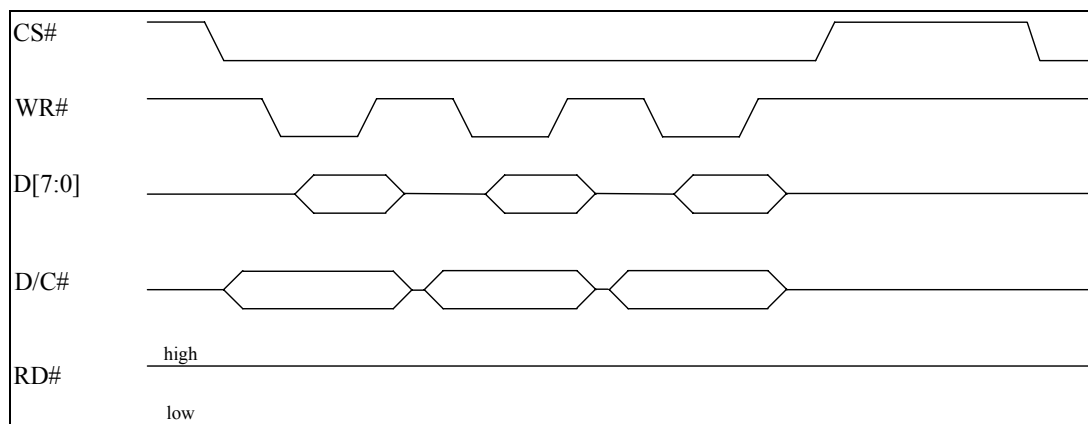
The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

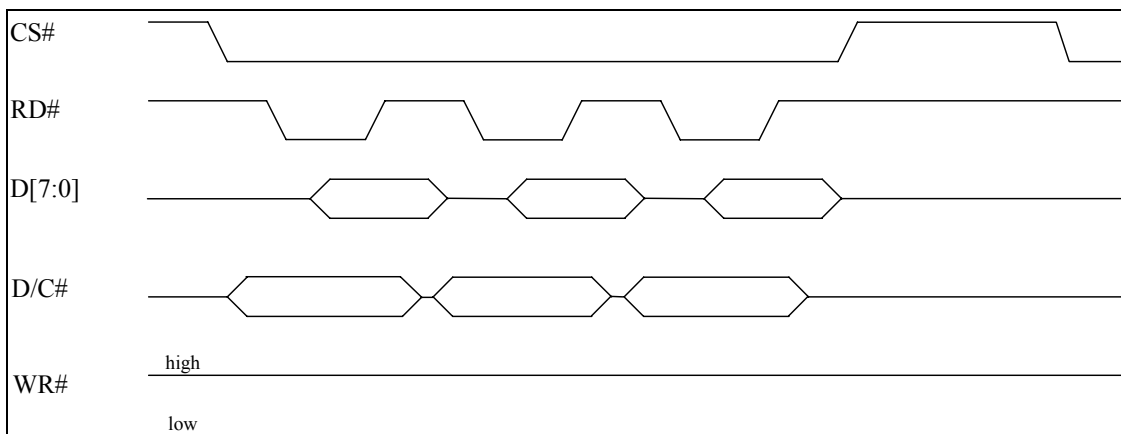
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

**Figure 8-2 : Example of Write procedure in 8080 parallel interface mode**



**Figure 8-3 : Example of Read procedure in 8080 parallel interface mode**





**Table 8-3 : Control pins of 8080 interface**

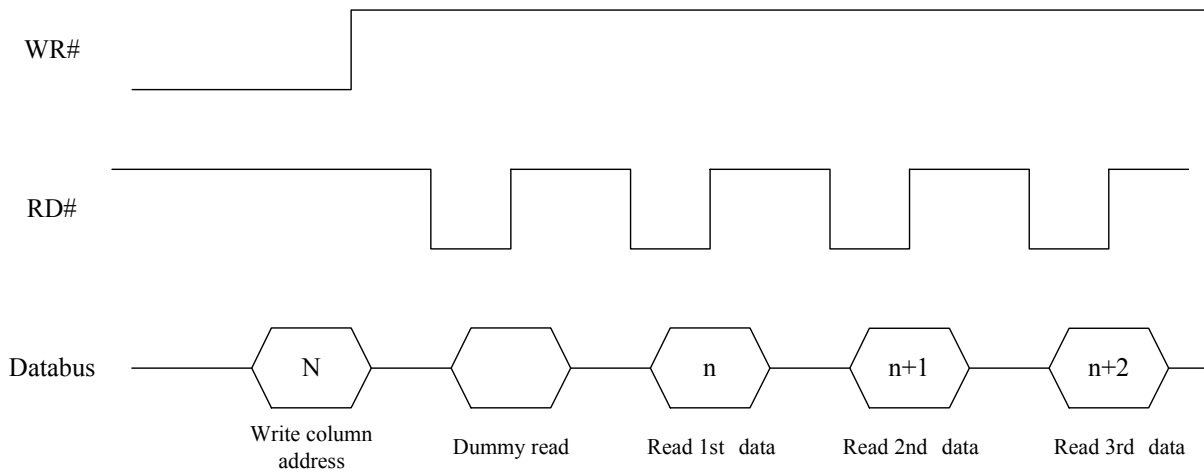
| Function      | RD# | WR# | CS# | D/C# |
|---------------|-----|-----|-----|------|
| Write command | H   | ↑   | L   | L    |
| Read status   | ↑   | H   | L   | L    |
| Write data    | H   | ↑   | L   | H    |
| Read data     | ↑   | H   | L   | H    |

**Note**

- (1) ↑ stands for rising edge of signal
- (2) H stands for HIGH in signal
- (3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

**Figure 8-4 : Display data read back procedure - insertion of dummy read**



### 8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#)# can be connected to an external ground.

**Table 8-4 : Control pins of 4-wire Serial interface**

| Function      | E(RD#)  | R/W#(WR#) | CS# | D/C# | D0 |
|---------------|---------|-----------|-----|------|----|
| Write command | Tie LOW | Tie LOW   | L   | L    | ↑  |
| Write data    | Tie LOW | Tie LOW   | L   | H    | ↑  |

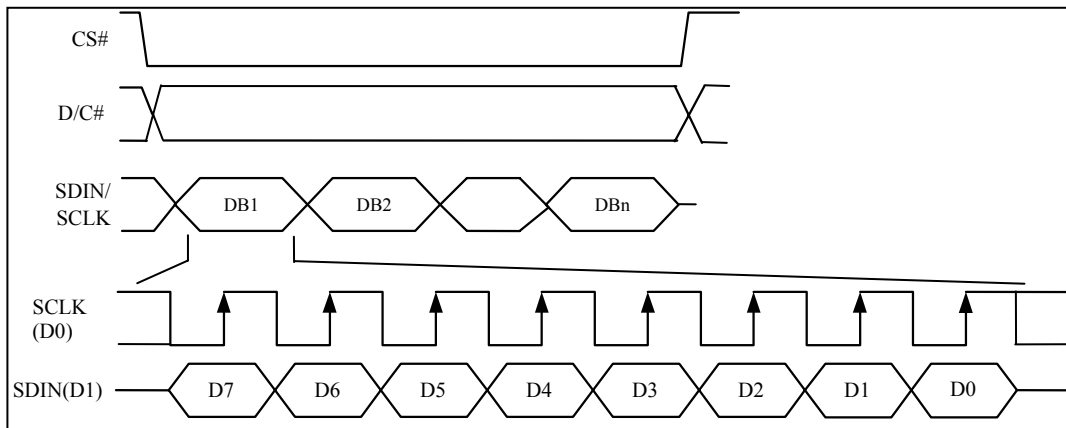
**Note**

- (1) H stands for HIGH in signal
- (2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

**Figure 8-5 : Write procedure in 4-wire Serial interface mode**



### 8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

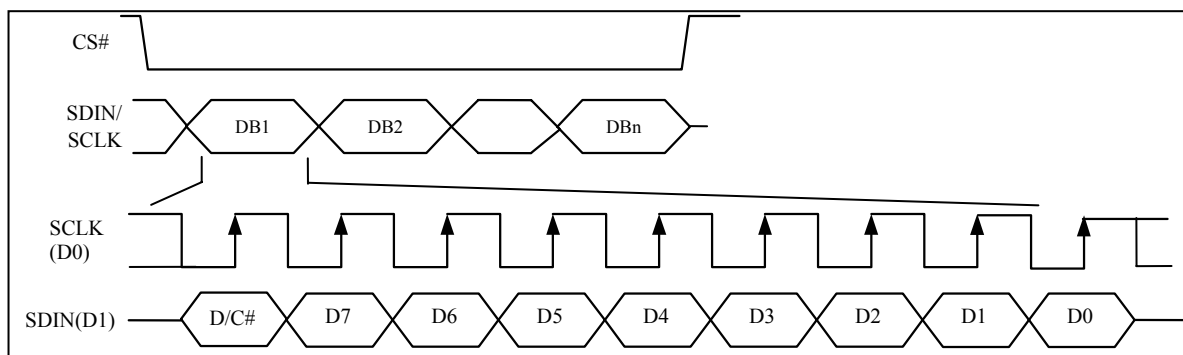
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

**Table 8-5 : Control pins of 3-wire Serial interface**

| Function      | E(RD#)  | R/W#(WR#) | CS# | D/C#    | D0 |
|---------------|---------|-----------|-----|---------|----|
| Write command | Tie LOW | Tie LOW   | L   | Tie LOW | ↑  |
| Write data    | Tie LOW | Tie LOW   | L   | Tie LOW | ↑  |

**Note**  
<sup>(1)</sup> L stands for LOW in signal

**Figure 8-6 : Write procedure in 3-wire Serial interface mode**



### 8.1.5 MCU I<sup>2</sup>C Interface

The I<sup>2</sup>C communication interface consists of slave address bit SA0, I<sup>2</sup>C-bus data signal SDA (SDA<sub>OUT</sub>/D<sub>2</sub> for output and SDA<sub>IN</sub>/D<sub>1</sub> for input) and I<sup>2</sup>C-bus clock signal SCL (D<sub>0</sub>). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)

SSD1306 has to recognize the slave address before transmitting or receiving any information by the I<sup>2</sup>C-bus. The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format,

b<sub>7</sub> b<sub>6</sub> b<sub>5</sub> b<sub>4</sub> b<sub>3</sub> b<sub>2</sub> b<sub>1</sub> b<sub>0</sub>

0 1 1 1 1 0 SA0 R/W#

“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101”, can be selected as the slave address of SSD1306. D/C# pin acts as SA0 for slave address selection.

“R/W#” bit is used to determine the operation mode of the I<sup>2</sup>C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I<sup>2</sup>C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at “SDA” pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in “SDA”.

“SDA<sub>IN</sub>” and “SDA<sub>OUT</sub>” are tied together and serve as SDA. The “SDA<sub>IN</sub>” pin must be connected to act as SDA. The “SDA<sub>OUT</sub>” pin may be disconnected. When “SDA<sub>OUT</sub>” pin is disconnected, the acknowledgement signal will be ignored in the I<sup>2</sup>C-bus.

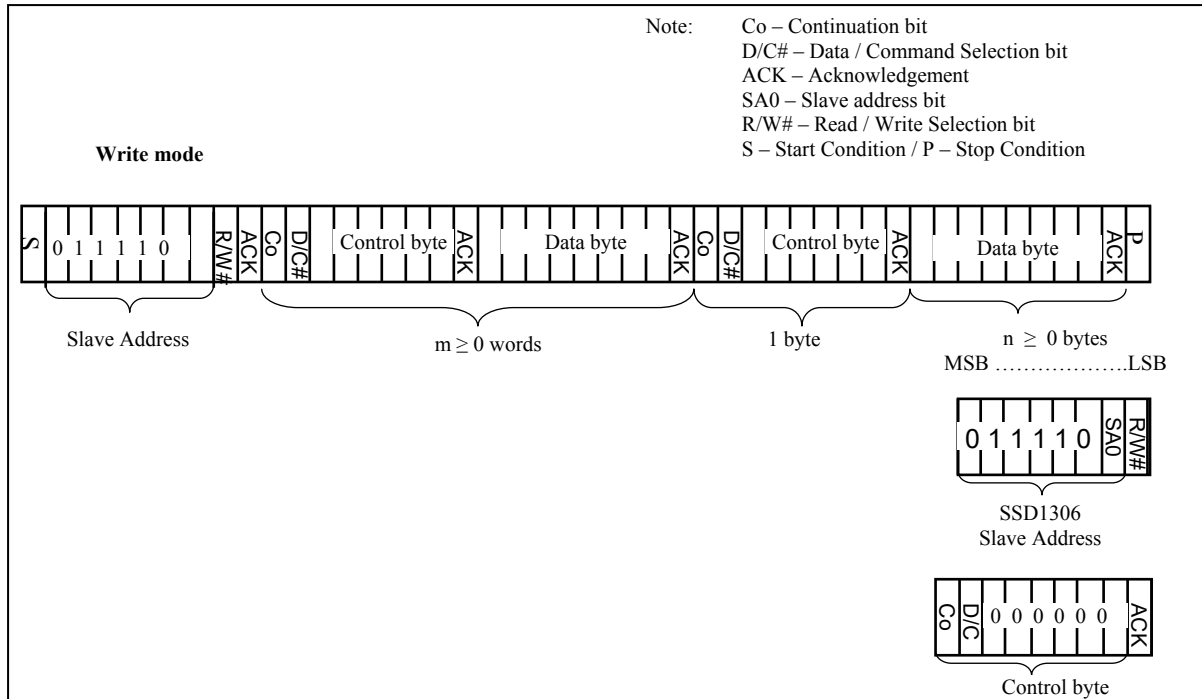
c) I<sup>2</sup>C-bus clock signal (SCL)

The transmission of information in the I<sup>2</sup>C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

### 8.1.5.1 I<sup>2</sup>C-bus Write data

The I<sup>2</sup>C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I<sup>2</sup>C-bus in chronological order.

**Figure 8-7 : I<sup>2</sup>C-bus data format**



### 8.1.5.2 Write mode for I<sup>2</sup>C

- 1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
- 2) The slave address is following the start condition for recognition use. For the SSD1306, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
- 3) The write mode is established by setting the R/W# bit to logic “0”.
- 4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
- 5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0”’s.
  - a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
  - b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
- 6) Acknowledge bit will be generated after receiving each control byte or data byte.
- 7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.